CLAIMS

1. A data processing arrangement (1) comprising:
- a first processor (PROC1) for providing successive sets of input data;
- a second processor (PROC2) for receiving successive sets of output data;
- a memory system (2) comprising a plurality of memory circuits (MEM) for receiving the successive sets of input data and providing the successive sets of output data,

wherein
- the data processing arrangement further comprises a master controller (MCP) for setting up the memory system by means of control commands (CC) associated with a set of input data and a set of output data;
- the memory system further comprises a control unit (MCU):
  - for, on the basis of the control commands, selecting a first memory circuit and generating a write-address (AD_W) in said first memory circuit when a data (Di) from the set of input data is provided by the first processor, and
  - for, on the basis of the control commands, selecting a second memory circuit and generating a read-address (AD_R) in said second memory circuit when a data (Do) from the set of output data is required by the second processor.

2. A data processing arrangement, as claimed in claim 1, wherein the control unit comprises:
- a write-counter (CNT_W) whose value is modified in association with a data received from the set of input data and which value indicates the write-address of the data in said first memory circuit;
- a read-counter (CNT_R) whose value is modified in association with a data provided from the set of output data and which value indicates the read-address of the data in said second memory circuit.

3. A data processing arrangement, as claimed in claim 1, wherein the control unit comprises a write-input port (7) for receiving a write-data signal (NXT_W) from the first processor in response to which the control unit generates the write-address and the control unit further comprises a read-input port (8) for receiving a read-data signal (NXT_R) from the second processor in response to which the control unit generates the read-address.

4. A memory system (2) comprising a plurality of memory circuits (MEM) for receiving successive sets of input data and for providing successive sets of output data, wherein the memory system further comprises a control unit (MCU) being programmable by means of control commands (CC) associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a

write-address (AD_W) in said first memory circuit, when a data (Di) from the set of input data is received, and for selecting a second memory circuit and generating a read-address (AD_R) in said second memory circuit, when a data (Do) from the set of output data is provided.

5. A method of processing data in a data processing arrangement (1) comprising:
- a first processor (PROC1) for providing successive sets of input data;
- a second processor (PROC2) for receiving successive sets of output data;
- a memory system (2) comprising a plurality of memory circuits (MEM) for receiving the successive sets of input data and providing the successive sets of output data,

wherein the method comprises, for a set of input data and a set of output data, the following steps:
- a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data;
- an execution step in which, on the basis of the control commands, the memory system:
  - selects a first memory circuit and generates a write-address in the first memory circuit for a data belonging to the set of input data;
  - selects a second memory circuit and generates a read-address in the second memory circuit for a data belonging to the set of output data.

"Data processing arrangement and memory system"

A data processing arrangement (1) comprises a first processor (PROC1) for providing successive sets of input data, a second processor (PROC2) for receiving successive sets of output data and a memory system (2) comprising a plurality of memory circuits (MEM) for storing the input and output data. According to the invention, the data processing arrangement further comprises a master controller (MCP) for setting up the memory system by means of control commands (CC) associated with a set of input data and a set of output data. These control commands are received in the memory system by a control unit (MCU). When a data (Di) from the set of input data is provided by the first processor, this control unit selects, on the basis of the control commands, a first memory circuit and generates a write-address (AD_W) in said first memory circuit. In the same way, when a data (Do) from the set of output data is required by the second processor, the control unit, on the basis of the control commands, selects a second memory circuit and generates a read-address (AD_R) in said second memory circuit. Thus, there is no need for the processors to provide addresses when they require or send data therefore leading to a simple data processing arrangement.

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